**In the Claims:**

**Please enter the following amended claims 8, 9, 15, 16, 20 and 21:**

8. (Twice Amended) A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type;

a gate insulating layer situated over said substrate, the gate insulating layer having a first thickness situated over said first region and said second region, and a second thickness situated over said third region, said first thickness being greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform; and

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a control gate situated over said gate insulating layer.

9. (Twice Amended) A memory cell comprising:

a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type; and

a gate insulating layer situated over said substrate, the gate insulating layer having a first thickness situated over said first region and said second region, and a second thickness situated over said third region, said first thickness being greater than said second thickness, wherein said first thickness is substantially uniform and said second thickness is substantially uniform; and

an ONO stack situated over said gate insulating layer.

15. (Amended) A memory cell as in claim 8, wherein an injection field in an overlap region situated between said gate insulating layer and said first and second regions ranges between approximately 4 Mv/cm and approximately 6 Mv/cm.

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16. (Amended) A memory cell as in claim 8, wherein an injection field in an overlap region situated between said gate insulating layer and said third region ranges between approximately 8 Mv/cm and approximately 11 Mv/cm.

20. (Amended) A memory cell as in claim 9, wherein an injection field in an overlap region situated between said gate insulating layer and said first and second regions ranges between approximately 4 Mv/cm and approximately 6 Mv/cm.

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21. (Amended) A memory cell as in claim 9, wherein an injection field in an overlap region situated between said gate insulating layer and said third region ranges between approximately 8 Mv/cm and approximately 11 Mv/cm.